



An Overview of Switching Scheme used in Multilevel Inverter

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Abstract- Inverter is a device which is used for converting DC power into AC. The basic constitute of all inverter is power switch. All switches are based on the gate pulse. The technique used for on or off the switches is call firing of the switch. There are many techniques used for the getting the switching. In this paper here discuss first the different types of topology used in the inverter and then discuss the different type of switching pulse width modulation used by the different researchers. This is the review paper which gives the overview of the work behind the multilevel inverter topology.

Keywords:- DC to Ac, MLI, H-Bridge inverter, PWM, SHEPWM.

Introduction

In an industrialized nation today, an increasingly significant portion of the generated electrical energy is processed through power electronics for various applications in industrial, commercial, residential, aerospace and military environments. The technological advances made in the field of power semiconductor devices over the last two decades, have led to the development of power semiconductor devices with high power ratings and very good switching performances. Also, the development of microprocessors and microcomputer technology has had a great impact on the control strategy for the power semiconductor devices. Some of the popular power semiconductor devices available in the

market today include Power MOS Field Effect Transistors (Power MOSFETs), Insulated Gate Bipolar Transistors (IGBTs) and Gate Turn Off Thyristors (GTOs). As a result of these rapid advancements in power semiconductor technology, substantial amount of research is being devoted to the area of static power converters. The input and output currents and voltages of static power converters are generally associated with harmful low-order harmonics.

Recently multilevel inverters are getting wide acceptance because of its superior features such as high quality voltage with very low distortion, reduced dv/dt stress and reduced electromagnetic interference. The concept of multilevel inverter is to achieve higher power conversion with series of power semiconductor switches connected to low voltage dc sources, such that the switching produces high quality staircase voltage waveform. Quality of power increases with higher voltage levels, but it may result in increased number of power electronic switches which in effect increases cost, control complexity and reduces overall efficiency.

In this review paper discuss in the next section II literature review based on the multi-level inverter. Section III is discuss the different pulse width modulation is used in the multilevel inverter. The basic problem is also discussed in the section IV.



II. Review of MLI

The first multi-level inverter is discussed in [1] which introduced the concept of multilevel inverters. They proposed the three or more level inverter is called multilevel inverter. Later on in 1981, the author proposed NPC MLI which produce three level output. He assumed that the medium voltage of the three level inverter as neutral point. After that the invention of multilevel is started. Various topologies regarding multilevel inverter are discussed [2]. This developed the basic contents like qualities, applications of multilevel inverters for high power. Because of generation of voltage level in multilevel inverter by translating dc voltage levels into multiple ac voltages, these are in more demanded to use in the high power applications. Multilevel inverter uses dc source of voltages for incorporating voltage waveform with stair case approach and reduces harmonic contents. The series inverter concept is developed from the use of H-bridge [3]. The aim was behind was that multiple voltages can be generated with the series connection of one phase inverter. With the help of this concept of series inverter connection had proposed the inverter topology known as cascaded H-bridge multilevel inverter [4]. Cascaded inverter was fully implemented for reactive power compensation in the high power applications [5]. It was instantly linked in series with the electrical system. For the application of the large electric drive is analysed [6]. They proved that cascaded H-bridge inverter is superior to be used in electric drive applications as these inverters use many separate dc sources which make it possible to achieve high ratings of power. With the connection of 5 level the 15 level output is produced [7]. The aim through this thought was to suggest that high number of voltage levels could be generated by the series connection of many H-bridges each having dc source voltage and approximate number of voltage steps. First realized symmetric seven level and fifteen level cascaded H-bridge inverter in [8]. The idea was to mitigate harmonics related problem in multilevel inverter. A comparative analysis is done for cascaded H-Bridge inverter with other topology present in [9]. In this paper

modified symmetric converter for utilizing in the high power and medium voltage applications present. Due to limitation of the symmetric inverters the type of cascaded H-bridge multilevel inverter is introduced through this work known as asymmetric configuration of cascaded H-bridge inverter which uses unequal dc voltages. The researcher suggested the idea of using asymmetrical inverter because with symmetric multilevel inverter, many sources of dc have to be used along with so many switches, but with asymmetric structure for generating the same number of voltage levels, less switching devices and dc sources are needed which give cost effective solution over symmetric arrangement of the inverter. With less number of switches, high voltage levels can be achieved with asymmetric inverters. So, from this research work, concept of asymmetrical cascaded H-bridge multilevel inverter was introduced. The realization of asymmetrical multilevel inverter is done in [10]. This can do by the help of comparison analysis on the basis of switching components, dc sources, and switch losses. Using five and seven level, a comparison was done. In [12] proposed different algorithms for selecting the values of separate dc sources. These methods give independency for designing any number of asymmetric voltage levels. Further proposed a new method for determine the values of dc voltages and inserted in the asymmetric arrangement of the inverter with using only three switching components and dc sources for achieving absolute number of levels [13]. The choice of the arrangement was dependent on the analysis of requirement of reduced switching devices, dc source voltages and decrement in dv/dt stresses for attaining high voltage levels. The description about the cascaded topology in which two H-bridges were incorporated with different frequency operation is discussed in [14]. The inverter was implemented in symmetric arrangement with one H-bridge administered at frequency high and another one was at fundamental which is at 50 Hz frequency for producing five levels of ac output voltage. The performance analysis of three phase seven level asymmetrical MLI at different modulation indices



is presented in [15]. The author made variations in the modulation index so as to reach the value of minimum THD. This is successfully achieved in this research work? The advantages of the proposed topology are revealed in this work as asymmetrical inverters are meant for using less switching components and individual dc sources. Binary based asymmetrical inverter is reported in [16]. In this two H-bridges are used in the inverter to make output voltage of seven levels. Both the H-bridges are made to operate at different values of frequencies. The author [17-18] discusses the comparative investigation between various levels of asymmetrical topology on the basis of losses in the switches, harmonic contents. These inverters operated at low frequency. For proving the superiority of asymmetrical cascaded H-bridge inverters over symmetrical inverter, performance of 15 level asymmetrical inverter is in the binary ratio is reported in paper [19]. The topology uses three H-bridges. Paper [20] presents the proposed method for selecting values for dc voltages for the asymmetrical inverter topology. The main objective of the proposed topology is to reflect the less IGBT switches and reduced cost. In paper [21], a reduced topology of asymmetrical cascaded H-bridge multilevel inverter is proposed. In this paper, it is shown that more number of voltage levels can be attained even with the reduced switch components; the paper also discusses the different algorithms such as binary, ternary for the calculation of separate dc sources. In this paper, ternary based asymmetrical cascaded H-bridge inverter is proposed. For producing 13 levels of voltages with using reduced topology is presented in paper [22]. In this paper, four dissimilar dc voltage sources are used with 10 switches. The topology is cascaded sub-multicell in which asymmetric configuration is possible to be implemented. The performance of the proposed topology comes out to be good and it satisfies the harmonic limits that is less than 5%.

III. Review on Multicarrier PWM for MLI

Pulse width modulation is the scheme used for gating the signal for power switches used in the multilevel inverter which is discussed in previous

chapter. This help to control the switch to produce multilevel output with the DC source. Here in this section discuss the basic modulation scheme used now a day for controlling of switch used in the multilevel inverter. For triggering the multilevel inverter sun-harmonic PWM strategy is discussed in [23]. For the high frequency applications, sub-harmonic PWM methods are effective to use. In order to overcome the demerits of pulse generator or any other PWM controller, concept of sub-harmonic control method was introduced for giving better reduced results of THD. First utilized the multi-carrier control strategy in single phase five level cascaded inverter for reduction of harmonics is discussed in [24]. One reference signal is compared with four triangular carrier signals. The researcher carried out the performance of multi-carrier method. The multi-carrier is based on a sinusoidal PWM strategy. Multi carrier method being implemented for both symmetrical and asymmetrical cascaded H-bridge multilevel inverter to limit THD is discussed in [25]. In this paper three different types of multi carrier method were proposed namely level shifted, similar switching frequency, different frequency and phase shifted method were introduced. Five different multi carrier sinusoidal PWM control strategies namely level shifted based fixed frequency Phase Disposition, Phase Opposition Disposition, Alternate Phase Opposition Disposition multicarrier PWM, Variable frequency and Phase shifted are studied in paper [26]. For the comparative analysis between all these methods of PWM, there are realized in five level cascaded H-bridge inverter. In order to find the superiority of asymmetrical as well as symmetrical cascaded multilevel inverters, when performed with the entire five carrier based PWM strategies, paper [27] presents the comparative test between the two topologies of MLI with all these PWM control methods. The results conclude that asymmetrical inverter gives very less THD. Work given in [28] showed that SHE could be implemented with a staircase modulation scheme working at a switching frequency equal to the converter output voltage fundamental frequency. In this scheme a



waveform with seven levels and three switching points per quarter cycle gave three degrees of freedom. One was used to ensure that the required fundamental value was achieved in the multilevel waveform whilst the other two were used to ensure that the 5th and 7th harmonics were eliminated. Unfortunately in this case, since the waveform was stepped, there were imbalances in the conduction times for each converter cell. To alleviate this cell conduction time switching scheme was utilized to ensure balance over several cycles. A method of producing multilevel SHE was shown in [29] where switching angles for a single H-Bridge were taken and phase shifted for an N level converter to achieve an initial guess for a multilevel set of equations. In this case a multilevel scheme with a 250Hz device switching frequency was achieved and multiple solutions were reduced by adding a reduced distortion objective function. Due to the imbalance in individual cell conduction blocks a cell swapping scheme was required. Work shown in [30] attempted to alleviate the requirement of a cell swapping scheme by better utilizing the degrees of freedom. In this case each cell of a seven level converter had three degrees of freedom (150Hz device switching frequency), giving a total of nine degrees of freedom. Six of these were used to eliminate the lowest order dominant harmonics whilst the final three were used to ensure that the fundamental component of each cell waveform was equal. This use of the degrees of freedom ensured that for an undistorted current flowing from the converter, the power drawn from each cell would be equal. Work by [31] used a 250Hz switching frequency scheme in conjunction with extra cells using a high switching frequency to eliminate both lower and higher order harmonics. This results in the production of very high quality waveforms. Disadvantages due to the high switching frequency of this extra cell resulted in an update to this work [32] whereby a lower switching frequency method was used to remove these higher order harmonics.

IV. Problem Statement

The problem of eliminating harmonics in switching converters has been the focus of

research for many years. Present day available PWM schemes can be broadly classified as carrier modulated sine PWM and pre-calculated programmed pulse width modulation (PPWM) schemes. If the switching losses in an inverter are not a concern (i.e., switching on the order of a few kHz is acceptable), then the sine-triangle PWM method and its variants are very effective for controlling the inverter.

This is because the generated harmonics are beyond the bandwidth of the system being actuated and therefore these harmonics do not dissipate power. On the other hand, for systems where high switching efficiency is of utmost importance, it is desirable to keep the switching frequency much lower. In this case, another approach is to choose the switching times (angles) such that a desired fundamental output is generated and specifically chosen harmonics of the fundamental are suppressed. This is referred to as selective harmonic elimination or programmed harmonic elimination as the switching angles are chosen (programmed) to eliminate specific harmonics. This is also called as Computed Pulse Width Modulation (CPWM) or Programmed Pulse Width Modulation (PPWM). The Programmed PWM techniques optimize a particular objective function such as to obtain minimum losses, reduced torque pulsations, selective elimination of harmonics and therefore the most effective means of obtaining high performance results. It is interesting to note that the various objective functions are chosen to generate a particular programmed PWM technique essentially constitutes the minimization of unwanted effects due to the harmonics present in the inverter output spectra.

In view of this, little or no difference between each one of the programmed techniques is observed when significant number of low order harmonics is eliminated. However, each one of the programmed PWM techniques is associated with the difficult task of computing specific PWM switching instants to optimize a particular objective function. This difficulty is particularly encountered at lower



output frequency range due to the necessity of large number of PWM switching instants. Also in most cases only a local minimum can be obtained after considerable computational effort.

V. Conclusion

For Dc power conversion inverter play major role. Due to high harmonics in the 2level inverter it is replaced by multilevel inverter now a day. In the multilevel inverter number of switch is increases which also produce harmonics. In this paper discuss the literature based on the multilevel inverter used in the industrial application. Also in this discuss the recent PWM scheme used for triggering of the switches present in the multilevel inverter. The basic proble associated in the use of switches in the multilevel inverter is also discussed.

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