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Performance Analysis of Selective Harmonic Elimination Pulse Width Modulation Based Single Phase Voltage Source Inverter

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Abstract- *Unwanted currents or voltages are known as harmonics. They can be found at frequencies that are a multiple or fraction of the fundamental frequency. In static power converters, harmonic pollution is a big concern. The type and control scheme of the converter decide the harmonic orders and magnitudes. The output voltage waveform of a single-phase voltage-source inverter is usually composed only of odd harmonics. They also harmonics are absent due to the half-wave symmetry of the output voltage harmonics. The triplen (third and multiples of third harmonics) are absent in three-phase voltage-source inverters, in addition to the even harmonics. The technique of selective harmonic elimination pulse width modulation (SHE-PWM) is discussed in this article. This technique is used to exclude chosen dominant low order harmonics from the output voltage of a multi-level inverter. The whole model is simulated in MATLAB software and the SHE PWM is applied on the single phase inverter topology.*

Keywords:- DC to Ac, MLI, H-Bridge inverter, PWM, SHEPWM.

Introduction

Power electronics processes a growing portion of the electrical energy produced in an industrialised nation today for numerous applications in manufacturing, commercial, domestic, aerospace, and military environments. Over the last two decades, technical developments in the field of power semiconductor devices have resulted in the production of power semiconductor devices with high power levels and very good switching outputs. Furthermore, the advancement in microprocessor and microcomputer technologies has had a major effect on the power semiconductor system control strategy. Power MOS Field Effect Transistors (Power MOSFETs), Insulated Gate Bipolar Transistors (IGBTs), and Gate Turn Off Thyristors are some of the most common power semiconductor devices on the market today (GTOs). As a result of these rapid advances in power semiconductor technologies, a significant amount of study is being dedicated to static power converters. Static power converter input and output currents and voltages are often associated with dangerous low-order harmonics.

Multilevel inverters have recently gained popularity due to their superior features such as high quality voltage with very low distortion, reduced dv/dt tension, and reduced electromagnetic interference. The idea behind a multilevel inverter is to achieve higher power transfer by connecting a series of power semiconductor switches to low voltage dc sources, resulting in a high quality staircase voltage waveform. Higher voltage levels improve power quality, but they can result in an increase in the number of power electronic switches, which raises

costs, increases control complexity, and decreases overall performance.

II. Background of MLI

The first multi-level inverter topology which introduced the idea of multilevel inverters is discussed in [1]. They proposed the term "multilevel inverter" for inverters of three or more levels. Later that year, in 1981, the author suggested NPC MLI, which generates three levels of production. He assumed that the neutral point of the three-level inverter was the medium voltage. Following that, the multilevel innovation process begins [2]. Various topologies for multilevel inverters are discussed. This established the fundamental contents such as the qualities and applications of multilevel inverters for high strength. Since multilevel inverters generate voltage levels by converting dc voltage levels into multiple ac voltages, they are increasingly in demand for use in high power applications. Multilevel inverter incorporates voltage waveform with stair case approach and reduces harmonic contents by using dc voltage source. The definition of a sequence inverter is derived from the usage of an H-bridge [3]. The aim was to produce multiple voltages using a series relation of a single phase inverter. With the support of this definition of series inverter interaction, he proposed the cascaded H-bridge multilevel inverter [4]. In high power applications, a cascaded inverter was completely introduced for reactive power compensation [5]. It was immediately connected to the electrical grid in series. The use of a massive electric drive is investigated [6]. They demonstrated that a cascaded H-bridge inverter is superior for use in electric drive applications since these inverters use several different dc sources, allowing them to achieve high power ratings. The production of 15 levels is provided by connecting 5 levels [7]. The aim of this thinking was to propose that a large number of voltage levels could be produced by connecting several H-bridges in sequence, each with a dc source voltage and an estimated number of voltage steps. In [8,] the first symmetric seven-level and fifteen-level cascaded H-bridge inverter was realised. The goal was to alleviate harmonics-related issues in multilevel inverters. In [9], a comparison of cascaded H-Bridge inverters with other topologies is performed. This paper presents a revamped symmetric converter for use in high power and medium voltage applications. Due to the limitations of symmetric inverters, this work introduces a type of cascaded H-bridge multilevel inverter known as an asymmetric configuration of cascaded H-bridge inverter that uses unequal dc voltages. The researcher proposed using an asymmetrical inverter since a symmetric multilevel inverter requires many dc sources as well as many switches, while an asymmetric structure requires less switching devices and dc sources to generate the same number of voltage levels, providing a more cost-effective alternative than a symmetric arrangement of the inverter. Asymmetric inverters can reach high voltage levels with a small number of switches. As a result of this study, the idea of asymmetrical cascaded H-bridge multilevel inverter was presented. [10] shows how to create an asymmetrical multilevel inverter. This can be accomplished by the use of a comparative analysis based on switching elements, dc sources, and switch losses. A contrast was made using the levels five and seven. Different algorithms for selecting the values of separate dc sources were proposed in [12]. These methods allow for the development of an infinite number of asymmetric voltage levels. Further suggested a new approach for determine the values of dc voltages and incorporated in the asymmetric structure of the inverter with using only three switching components and dc sources for achieving absolute number of levels [13] Formal paraphrase. The structure was chosen based on an appraisal of the need for decreased switching equipment, dc source voltages, and a decrease in dv/dt pressures in order to achieve high voltage values. [14] Discusses the cascaded topology in which two H-bridges with separate frequency operations is integrated. The inverter was implemented in a symmetric configuration with one H-bridge administered at high frequency and another at fundamental frequency, which is 50 Hz, for generating five levels of ac output voltage. [15]

Presents a performance study of three step seven stage asymmetrical MLI at various modulation indices. The author changed the modulation index to achieve the lowest possible THD. Is this accomplished in this research work? The benefits of the proposed topology are shown in this work because asymmetrical inverters are designed to use fewer switching components and individual dc sources. [16] describes a binary-based asymmetrical inverter. In this inverter, two H-bridges are used to generate output voltage with seven steps. Both H-bridges are designed to work at various frequencies. The reviewer [17-18] addresses a comparative investigation of different degrees of asymmetrical topology based on switch losses and harmonic contents. This inverters had a low frequency of operation. The efficiency of a 15 level asymmetrical inverter in the binary ratio is stated in paper [19] to demonstrate the supremacy of asymmetrical cascaded H-bridge inverters over symmetrical inverters. Three H-bridges are used in the topology. The suggested method for choosing dc voltage values for the asymmetrical inverter topology is presented in paper [20]. The suggested topology's key goal is to reflect fewer IGBT switches and lower costs. A simplified topology of an asymmetrical cascaded H-bridge multilevel inverter is proposed in paper [21]. In this article, it is shown that a greater number of voltage ranges can be achieved even with fewer switch components; the paper also addresses various algorithms such as binary and ternary for the computation of independent dc sources. A ternary-based asymmetrical cascaded H-bridge inverter is proposed in this article. The paper [22] presents a method for generating 13 degrees of voltage with a reduced topology. Four dissimilar dc voltage sources and ten switches are included in this paper. The topology is cascaded sub-multicell, with the ability to apply asymmetric configurations. The suggested topology performs well and meets the harmonic limits, which are less than 5%.

The scheme for gating the signal for power switches used in the multilevel inverter mentioned in the previous chapter is pulse width modulation. This aids in controlling the transition to generate multilevel output from the DC source. This section discusses the simple modulation scheme used today for manipulating the transition in a multilevel inverter. The sun-harmonic PWM technique is explored in [23] for activating the multilevel inverter. Sub-harmonic PWM approaches are useful for high frequency applications. To address the shortcomings of a pulse generator or some other PWM controller, the principle of sub-harmonic control was implemented in order to achieve better THD reduction performance. [24] discusses the first use of the multi-carrier control technique in a single step five stage cascaded inverter for harmonic reduction. Four triangular carrier signals are equivalent to one reference signal. The performance of the multi-carrier approach was carried out by the researcher. The multi-carrier strategy is based on sinusoidal PWM. [25] discusses the multi carrier approach for limiting THD in both symmetrical and asymmetrical cascaded H-bridge multilevel inverters. This paper presented three distinct types of multi carrier methods: level shifted, equivalent switching frequency, different frequency, and phase shifted. The paper [26] investigates five separate multicarrier sinusoidal PWM control mechanisms, including level shifted dependent fixed frequency Phase Disposition, Phase Opposition Disposition, Alternate Phase Opposition Disposition multicarrier PWM, Variable frequency, and Phase shifted. All of these PWM approaches are realised in a five-level cascaded H-bridge inverter for comparative study. Paper [27] provides a comparison test between the two topologies of MLI for all of these PWM control methods in order to determine the superiority of asymmetrical as well as symmetrical cascaded multilevel inverters as conducted with the full five carrier dependent PWM strategies. The findings show that an asymmetrical inverter produces very little THD. The study presented in [28] demonstrated that SHE could be applied using a staircase modulation scheme with a switching frequency equal to the fundamental frequency of the converter output voltage. A waveform with seven stages and three switching points per quarter cycle provided three degrees of freedom in this scheme. One was used

to ensure that the requisite fundamental value was obtained in the multilevel waveform, while the other two were used to remove the 5th and 7th harmonics. Unfortunately, since the waveform was stepped in this situation, there were imbalances in the conduction times for each converter cell. To address this, a cell conduction time switching scheme was used to maintain equilibrium over several cycles.[29] demonstrated a procedure for generating multilevel SHE by taking switching angles for a single H-Bridge and phase shifting for a N level converter to obtain an initial guess for a multilevel series of equations. A multilevel scheme with a system switching frequency of 250Hz was accomplished in this situation, and several solutions were minimised by using a minimised distortion objective feature. A cell swapping scheme was expected due to the imbalance in individual cell conduction blocks. The work seen in [30] sought to reduce the need for a cell switching system by making greater use of the degrees of freedom. Each cell of a seven-level converter in this case had three degrees of freedom (150Hz unit switching frequency), for a total of nine degrees of freedom. Six of these were used to exclude the lowest order dominant harmonics, while the other three were used to ensure that the fundamental aspect of each cell waveform was identical. The use of degrees of freedom meant that the power drawn from each cell would be equal with an undistorted current flowing from the converter. To remove all lower and higher order harmonics, [31] used a 250Hz switching frequency scheme in combination with extra cells using a high switching frequency. As a consequence, very high-quality waveforms are generated. Owing to the disadvantages of this extra cell's high switching frequency, this study was updated [32], and a lower switching frequency approach was used to eliminate these higher order harmonics.

III. Problem Statement

For several years, researchers have focused on the issue of removing harmonics in switching converters. There are two types of PWM schemes available today: carrier modulated sine PWM and pre-calculated programmed pulse width modulation (PPWM). If switching losses in an inverter are not a problem (i.e., switching on the order of a few kHz is acceptable), the sine-triangle PWM system and its derivatives are very useful for inverter power. But it is note removing the odd harmonics present in the power converter output. This is due to the fact that the induced harmonics are outside the bandwidth of the device being actuated, and hence do not dissipate power. In the other hand, in systems where switching performance is critical, it is preferable to maintain the switching frequency as low as possible. Another solution in this case is to choose the switching times (angles) such that a desired fundamental output is produced while suppressing precisely selected harmonics of the fundamental. Since the switching angles are selected (programmed) to eliminate individual harmonics, this is known as selective harmonic elimination or programmed harmonic elimination. Computed Pulse Width Modulation (CPWM) or Programmed Pulse Width Modulation (PPWM) is other names for this (PPWM). Programmed PWM strategies refine a certain target function, such as producing minimal losses, minimised torque pulsations, selective removal of harmonics, and thus the most efficient way of achieving high output outcomes. It is worth noting that the different objective functions used to produce a specific programmed PWM technique basically represent the minimization of unintended effects caused by harmonics in the inverter output spectra.

IV. Selective Harmonics Elimination For 1 Phase VSI

The Power Electronics Research facility's ongoing research is mainly focused on optimum PWM strategies for harmonic reduction in different power electronic circuits. The theory for a general optimal PWM scheme for harmonic reduction in various power electronic circuits was initially developed. The best PWM scheme was then extended to a single-phase current source ac to dc converter and tested successfully on the bench. Analyzing the two-state output waveform of a single-phase inverter results in the development of

a simplified procedure for potentially removing any number of harmonics. The simple square wave is chopped a number of times, and a fixed relationship is derived between the number of chops and the potential number of harmonics that can be omitted.

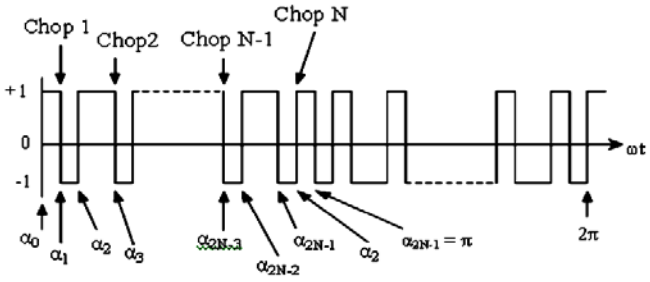

Fig 1: Generalized output waveform for single phase inverter

Actually, the SHE PWM technique is used to generate an output waveform for both a half-bridge and a full-bridge inverter. The power electronics inverter's generalized harmonic equation is:

$$V_{2k+1} = \frac{4V_{dc}}{(2k+1)\pi}\sum_{i=0}^{N} h_i \cos(2k+1)\alpha_i \quad [1]$$

Where, V is the output voltage of the inverter for V_{dc} dc input voltage, α is the switching firing angle of the system and $h_i$is the level of output. So by the help of Newton's method here find the firing angles for elimination of selective harmonics generated by the power converter

$$\cos(\alpha_1) - \cos(\alpha_2) + \ldots\ldots\ldots\ldots\ldots\ldots \pm \cos(\alpha_N) = \frac{\pi}{4}M \quad [2]$$

$$\cos(3\alpha_1) - \cos(3\alpha_2) + \ldots\ldots\ldots\ldots\ldots\ldots \pm \cos(3\alpha_N) = \frac{3\pi}{4}Mh_3 \quad [3]$$

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \ldots\ldots\ldots\ldots\ldots\ldots \pm \cos(5\alpha_N) = \frac{5\pi}{4}Mh_5 \quad [4]$$

$$\cos(N\alpha_1) - \cos(N\alpha_2) + \ldots\ldots\ldots\ldots \pm \cos(N\alpha_N) = \frac{N\pi}{4}Mh_N \quad [5]$$

Where, M is the modulation index and its value is $\frac{h_i}{V_{dc}}$

V. Simulation & Result

The harmonic elimination technique, as discussed in the previous section, is used in modern power inverters to turn the power switches. For validation, the whole work is simulated in the MATLAB programme. This work is focused on a single phase power inverter with a PWM technique based on selective harmonic elimination. The SIMULINK model for the proposed work is depicted in Figure 2.

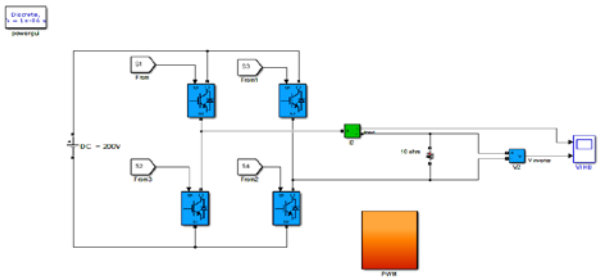

Fig 2: SIMULINK Model of Proposed VSI

The suggested PWM technique is tested using a single step voltage source inverter topology. The proposed work is motivated by the increasing use of non-conventional energy sources such as solar, fuel cells, and wind. As switches S1 and S4 are turned on, the inverter produces positive output, while switches S3 and S2 produce negative output. As a result, the switch gate configuration is more critical for the use of the voltage source inverter. Figure 3 depicts the fundamental SIMULINK model for producing the pulse of the proposed SHEPWM technique.

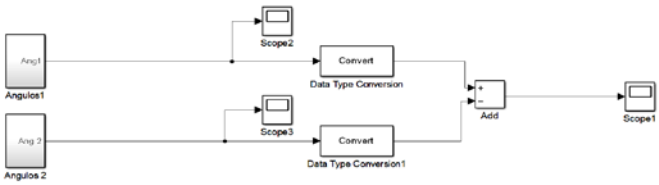

Fig 3: SIMULINK Model of proposed SHEPWM

Here, we use a resistive load with a DC input voltage of 200V to generate the result. The Newton-Rapshon method is used to pick the angle in this case. This technique generates five optimized angles for the intent of activating the inverter turn. The overall goal of the work is to reduce selective harmonics in the output. Lower order harmonics such as 1st, 3rd, 5th, 7th, and 9th

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order harmonics are removed from the output in this work. Figure 4 depicts the angle generated by the Newton-Raphson process.

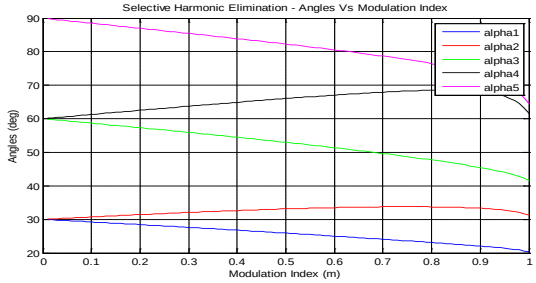

Fig 4: Angle v/s Modulation index of finding elimination angle

Figure 5 shows that the elimination angle varies with the modulation index of the device. At modulation index 90 percent, the optimised angle is a_1=22.0275, a_2=33.3203, a_3=45.4513, a_4=68.1123, and a_5=73.3370. The switching gate pulse for switches S_1 and S_4 and the switching gate pulse for switches S_2 and S_3 is shown in Figure 5.

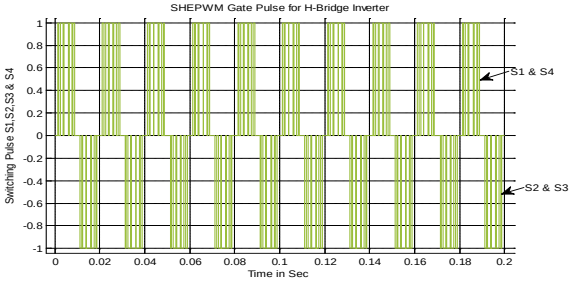

Fig 5: Switching pulse generated by proposed SHEPWM Technique

Figure 6 shows the output current when the voltage source inverter is loaded with resistive load. Figure 7 shows the FFT analysis of the current output.

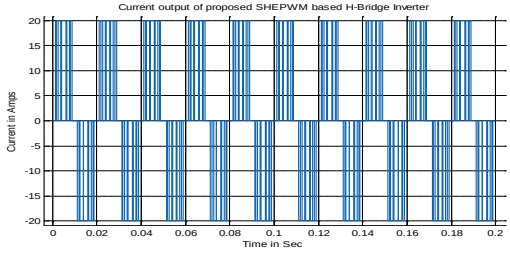

Fig 6: Current output of proposed SHE PWM based single phase VSI

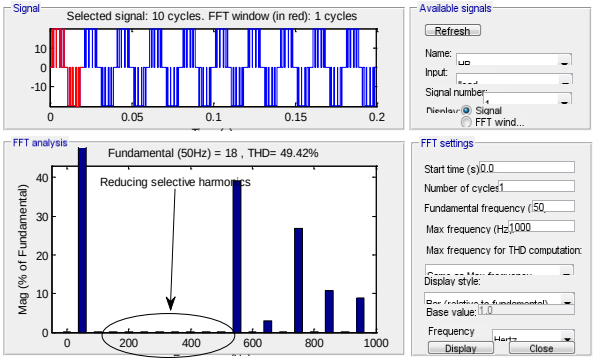

Fig 7: FFT Analysis of the output current for resistive load

VI. Conclusion

Harmonics are the system's undesired signal. It causes the machine to heat up, reducing power efficiency. Several technologies are currently being developed to exclude harmonics from the structure. Pulse width modulation is a technique for reducing harmonics in a device. This technique is used to transform the power converter's switches on and off. The selective harmonic elimination technique is used in this article. This paper also discusses the statistical analysis used to exclude selective harmonics. The 3rd, 5th, 7th, and 9th harmonics are attacked and eliminated here. The Newton-Raphson exclusion method was used in this case to exclude the chosen harmonics. The outcome demonstrates the exclusion of the chosen harmonics in the inverter topology.

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